GateMate™ FPGA

Suitable from small projects up to high volume applications

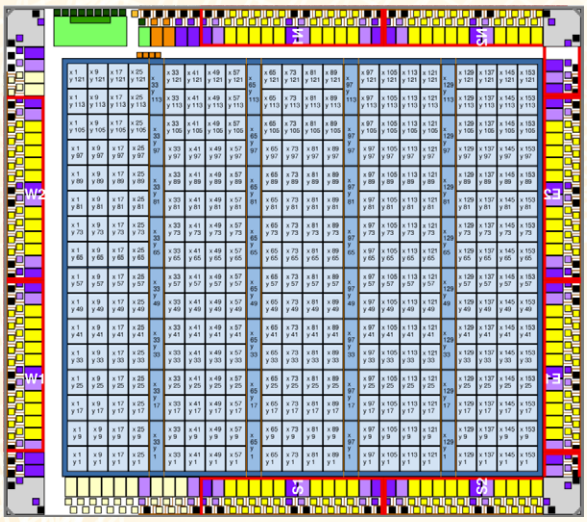
designed and manufactured in Germany

Overview

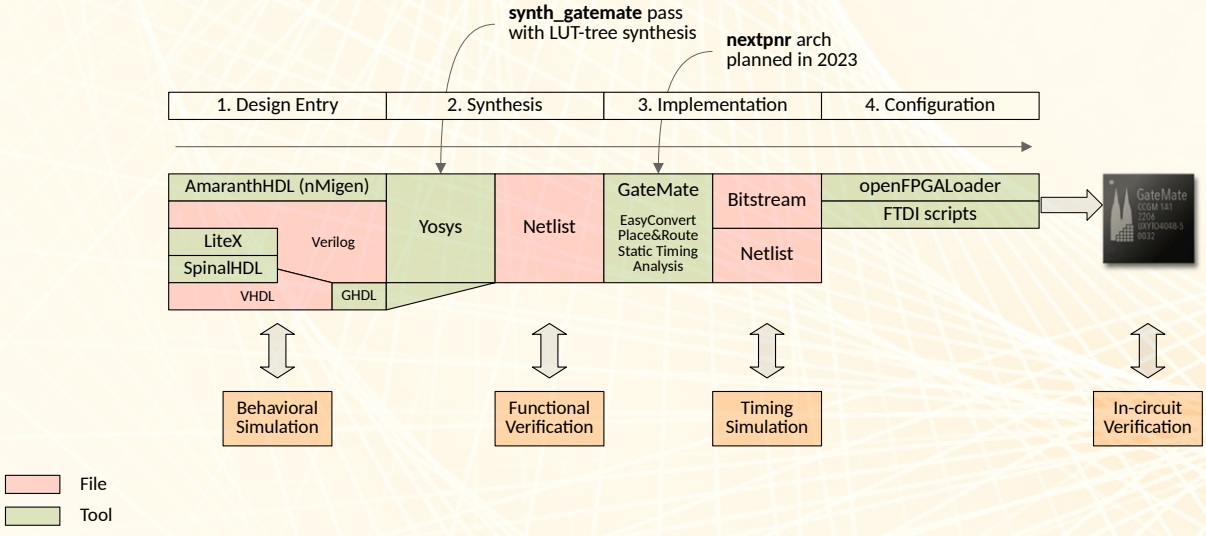
The GateMate FPGA family leverages the full breadth of Cologne Chip innovation and EU based manufacturing. High logic capacity with multi-die capability and low power footprint combined with lowest cost in industry make GateMate well suited for high volume applications.

The architecture of the GateMate FPGA is based on a novel programmable element (Cologne Programmable Element). The CPE architecture allows an efficient building of arbitrarily sized logic, such as multipliers for digital signal processing applications. Applications can utilize embedded Block RAMs with bit widths from 1 to 80 bits. Fast communication can be realized with over 162 GPIO pins, which can be configured as single-ended or LVDS differential pairs, each of them supporting double data rate (DDR). The embedded Serializer-Deserializer (SerDes) blocks allow high-speed serial communication with bandwidths of up to 5 Gb/s.

The strengths of GateMate FPGA devices are reinforced by incorporating Open-Source design tools and a proprietary free of charge Place & Route tool by Cologne Chip into the design flow. By that, Cologne Chip taps into vast resource of innovation potential and enables easy start with GateMate FPGAs. The appeal of GateMate is rounded by utilizing reliable and advanced process nodes (Globalfoundries™ 28nm SLP) and by availability through EU based manufacturing.



Architecture overview of **GateMate™ CCGM1A1**



Design flow of **GateMate™**

Cologne Chip
GateMate FPGA

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GateMate FPGA Technology

Supported by:

Federal Ministry for Economic Affairs and Energy

on the basis of a decision by the German Bundestag

GateMate™ Features

- Logic capacity from 20,480 to 512,000 CPEs
- Block RAM from 1,310,720 to 32,768,000 bits
- 3 Operation Modes: low power (0.9V), economy (1.0V), speed (1.1V)
- Ball grid package for low size and high pin count, requiring only 4 layers on PCB
- Small configuration file and fast configuration by using Quad SPI interface (up to 100MHz)
- Embedded 5 Gb/s Serializer-Deserializer (SerDes)
- Multiple clock domains (from 4 to 100 embedded PLLs)
- Support for ADC and DAC with additional IPs
- No excessive start-up currents
- Globalfoundries™ 28nm Super Low Power (SLP) manufactured in Europe
- Yosys framework coupled with proprietary, free of charge, Place & Route tool
- GateMate is available in different variants and sizes with preserved main pin compatibility
- ITAR free

GateMate™ Evaluation Board

Interfaces:

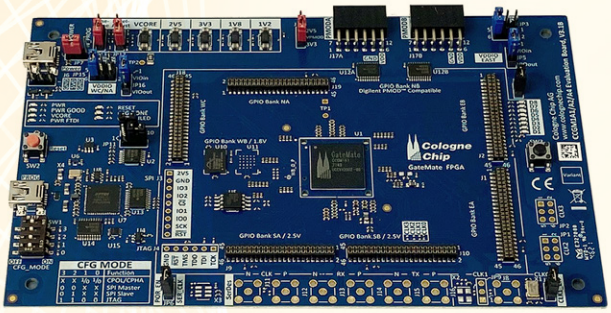
- Six I/O banks + access to SPI/JTAG signals
- Two standard 12-pin Pmod™ connectors
- 5 Gb/s SerDes via SMA connectors
- Access to all dedicated clock inputs
- Configuration via Flash on board, USB or JTAG

Memory:

- 64 Mbit Quad-I/O SPI Flash
- Up to two HyperBus memories on board (HyperRAM/HyperFlash)

Power:

- User-selectable core and I/O voltages



Evaluation Board of **GateMate™**

Device	Rel. size	Cologne Programmable Elements 1) 2)		Block RAM 3)		PLLs	SerDes	I/Os		Package		Availability
		CPEs	FF/Latches	20Kb	40Kb			single-ended	differential	balls	size (mm)	
CCGM1A1	1	20,480	40,960	64	32	4	1	162	81	324BGA	15x15	now
CCGM1A2	2	40,960	81,920	128	64	8	2	162	81	324BGA	15x15	now
CCGM1A4	4	81,920	163,840	256	128	16	4	154	77	324BGA	15x15	Q4 2023
CCGM1A9	9	184,320	368,640	576	288	36	9	tba	tba	tba	tba	tba
CCGM1A16	16	327,680	655,360	1,024	512	64	16	tba	tba	tba	tba	tba
CCGM1A25	25	512,000	1,024,000	1,600	800	100	25	tba	tba	tba	tba	tba

1) CPEs have 2x4 or 8 inputs connected to a LUT tree 2) Each CPE can be used as 2x2 Multiplier tile 3) Block RAM can have a data width of 1-80 bits

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